AMENDMENTS TO THE CLAIMS

1. (currently amended) A method for ~~writing data to~~ protecting a first boot area of a plurality of boot areas of a synchronous memory device, the method comprising:

initiating ~~a write~~ an erase operation to the first boot area;

reading data from a register circuit and detecting a security voltage; and

authorizing the ~~write~~ erase operation to the first boot area if the data is in a first state or ~~and~~ the security voltage exceeds a predetermined voltage.

2. (Previously presented) The method of claim 1 further comprising:
checking a status of a detection circuit if the data is in a second state; and
authorizing the write operation to the first boot area based on an output of the detection circuit.

3. (original) The method of claim 2 wherein the detection circuit monitors an externally provided signal applied to the memory device.

4. (Previously presented) The method of claim 1 wherein the plurality of boot areas comprise memory cells located at least significant and most significant addressable memory sectors of the synchronous memory device.

5. (currently amended) A memory device comprising:

an array of memory cells comprising a first and a second boot area;

a data register that stores protect status bits corresponding to a protect status of each boot area; and

a state machine capable of executing a method of ~~writing to~~ erasing each boot area including initiating ~~a write~~ an erase operation to either the first or the second boot area, reading the protect status bits from the data register, determining a voltage level of a security voltage, and authorizing the ~~write~~ erase operation to one of the first or the second boot area if the protect status bits are in a first state or the security voltage is greater than a predetermined voltage.

6. (currently amended) A memory device comprising:

an array of memory cells having a first and a second boot area;

a non-volatile data register that stores protect status bits indicating a protect status of the at least one boot area;

a volatile data register corresponding to the non-volatile data register such that the protect status bits are transferred from the non-volatile data register to the volatile data-register;

a security voltage input that provides a security function for the first and second boot areas; and

control circuitry coupled to the non-volatile and volatile registers and the security voltage input to selectively prevent erase ~~or write~~ operations from being performed on the at least one boot area in response to a state of the protect status bits and the voltage level of the security voltage.

7. (original) The memory device of claim 6 wherein the control circuitry is capable of transferring the protect status bits from the non-volatile data register to the volatile data register on power-up of the memory device.

8. (currently amended) A method for ~~writing data to~~ erasing a boot area of a plurality of boot areas of a memory device, the method comprising:

transferring a protect status bit from a non-volatile data register to a volatile data register;

initiating ~~a write~~ an erase operation to the boot area;

reading the protect status bit from the volatile data register; ~~and~~

reading a security voltage; and

authorizing the ~~write~~ erase operation to the boot area if the protect status bit is in a first state or the security voltage is greater than a predetermined voltage.

9. (original) The method of claim 8 wherein the protect status bit is transferred from the non-volatile data register to the volatile data register upon power-up of the memory device.

10. (Previously presented) The method of claim 8 and further including writing data to a second boot area of the plurality of boot areas when the first boot area no longer has sufficient capacity to hold additional data.